IN THE CLAIMS:

Please amend the claims as follows. The claims are in the format required by 35 C.F.R. § 1.121.

1-3. (Canceled)

4. (Currently amended) ~~The system of claim 3, further comprising~~ A system comprising:

a first set of storage locations;

a second set of storage locations; and

control logic including a state machine configured to

load data from a plurality of parallel data streams received according to a first clock signal having a first rate into the first set of storage locations,

allow values of the data to stabilize in the first set of storage locations,

load data from the first set of storage locations to the second set of storage locations,

read data from the second set of storage locations according to a second clock signal having a rate that is different from the rate of the first clock signal,

determine a delay between data being loaded into the first set of storage locations and the same data being loaded into the second set of storage locations, and

selectively add or drop data to maintain the delay in a predetermined range

delay logic configured to delay a load signal associated with the first set of storage locations and to provide the delayed load signal to the state machine.

5. (Original) The system of claim 4, wherein the state machine is configured to determine the delay between data being loaded into the first set of storage locations and being loaded into the second set of storage locations by delaying a load signal corresponding to a selected storage location in the first set by a predetermined amount and determining whether the delayed load signal falls within a temporal window associated with loading a selected storage location in the second set.

6. (Original) The system of claim 5, wherein the state machine is configured to selectively add or drop data by: if the delayed load signal falls within the temporal window, reading data sequentially out of the second set of storage locations; if the delayed load signal precedes the temporal window, skipping reading one of the second set of storage locations; and if the delayed load signal follows the temporal window, reading an additional one of the second set of storage locations.

7. (Currently amended) ~~The system of claim 1,~~ A system comprising:
a first set of storage locations, wherein the first set of storage locations comprises four storage locations and wherein each storage location is configured to store a bit from each of parallel data streams;
a second set of storage locations; and
control logic configured to
load data from a plurality of parallel data streams received according to a first clock signal having a first rate into the first set of storage locations,
allow values of the data to stabilize in the first set of storage locations,
load data from the first set of storage locations to the second set of storage locations,
read data from the second set of storage locations according to a second clock signal having a rate that is different from the rate of the first clock signal,
determine a delay between data being loaded into the first set of storage locations and the same data being loaded into the second set of storage locations, and
selectively add or drop data to maintain the delay in a predetermined range.

8. (Original) The system of claim 7, wherein the second set of storage locations comprises four storage locations corresponding to the storage locations in the first set, and an additional storage location, wherein adding data comprises reading the additional storage location.

9. (Canceled)

10. (Currently amended) ~~The system of claim 9~~ A system comprising:

a first set of storage locations;

a second set of storage locations; and

control logic configured to

load data from n parallel data streams received according to a first clock signal having a first rate into the first set of storage locations,

allow values of the data to stabilize in the first set of storage locations,

load data from the first set of storage locations to the second set of storage locations,

read data from the second set of storage locations according to a second clock signal having a rate that is different from the rate of the first clock signal,

determine a delay between data being loaded into the first set of storage locations and the same data being loaded into the second set of storage locations, and

selectively add or drop data to maintain the delay in a predetermined range,

wherein the second clock rate is n times the first clock rate.

11. (Original) The system of claim 10, wherein the control logic is configured to reading data from the second set of storage locations in an interleaved fashion to generate a single serial data stream at the second clock rate.

12. (Canceled)

13. (Currently amended) ~~The system of claim 12, wherein the control logic is configured to~~ A system comprising:

a first set of storage locations;

a second set of storage locations; and

control logic configured to

load data from a plurality of parallel data streams received according to a first clock signal having a first rate into the first set of storage locations,

allow values of the data to stabilize in the first set of storage locations,

load data from the first set of storage locations to the second set of storage locations,

read data from the second set of storage locations according to a second clock signal having a rate that is different from the rate of the first clock signal and discard every second bit,

determine a delay between data being loaded into the first set of storage locations and the same data being loaded into the second set of storage locations, and

selectively add or drop data to maintain the delay in a predetermined range.

14. (Canceled)

15. (Currently amended) ~~The method of claim 14, wherein determining the delay between each data bit being loaded into the first set of storage locations and the data bit being loaded into the second set of storage locations comprises:~~ A method comprising:

loading data received according to a first clock signal having a first rate into a first set of storage locations according to a first clock signal;

allowing values of the data to stabilize in the first set of storage locations;

loading data from the first set of storage locations to a second set of storage locations;

reading data from the second set of storage locations according to a second clock signal having a second rate that is different from the first rate;

determining a delay between each data bit being loaded into the first set of storage locations and the data bit being loaded into the second set of storage locations by delaying a load signal corresponding to a selected storage location in the first set by a predetermined amount[[;]] and determining whether the delayed load signal falls within a temporal window associated with loading a selected storage location in the second set; and

selectively adding or dropping data to maintain the delay in a predetermined range.

16. (Original) The method of claim 15, wherein selectively adding or dropping data to maintain the delay in a predetermined range comprises: if the delayed load signal falls within the temporal window, reading data sequentially out of the second set of storage locations; if the delayed load signal precedes the temporal window, skipping reading one of the second set of storage locations; and if the delayed load signal follows the temporal window, reading an additional one of the second set of storage locations.

17. (Canceled)

18. (Currently amended) ~~The method of claim 17, wherein the second clock rate~~ A method comprising:

loading data received in n parallel data streams according to a first clock signal having a first rate into a first set of storage locations according to a first clock signal;

allowing values of the data to stabilize in the first set of storage locations;

loading data from the first set of storage locations to a second set of storage locations;

reading data from the second set of storage locations according to a second clock signal having a second rate that is n times the first clock rate;

determining a delay between each data bit being loaded into the first set of storage locations and the data bit being loaded into the second set of storage locations; and

selectively adding or dropping data to maintain the delay in a predetermined range.

19. (Original) The method of claim 18, wherein reading data from the second set of storage locations comprises interleaving the data from the parallel data streams and generating a single serial data stream at the second clock rate.

20. (Canceled)

21. (Currently amended) ~~The method of claim 20, wherein every second bit is discarded~~ A method comprising:

loading data received according to a first clock signal having a first rate into a first set of storage locations according to a first clock signal;

allowing values of the data to stabilize in the first set of storage locations;

loading data from the first set of storage locations to a second set of storage locations;

reading data from the second set of storage locations according to a second clock signal having a second rate that is different from the first rate, discarding a portion of the data bits and generating a single serial data stream at a reduced clock rate;

determining a delay between each data bit being loaded into the first set of storage locations and the data bit being loaded into the second set of storage locations; and

selectively adding or dropping data to maintain the delay in a predetermined range.